FREQUENCY SYNTHESIZER DESIGN IN CMOS

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Abstract – *This paper presents design considerations for 4.19 MHz PLL frequency synthesizer with 32 kHz reference. Design of CMOS circuit with off-chip loop filter is presented. Also, an attempt is made to propose fully integrated design.*

1. INTRODUCTION

PLL is a circuit that synchronizes a reference (input) signal and feedback from its VCO (PLL output) so that signal and feedback can operate at the same frequency. In typical situation, both of the signals have some typical difference prior to the synchronization process. The time it takes the PLL to synchronize both signals into the same frequency and phase is referred to as "lock time". The main objective of the PLL is to obtain a locked state at a reasonable amount of lock time. Due its characteristics, PLL is used for communication systems and other circuits that require a clock recovery circuits, frequency multiplier, and data synchronization.

The paper is organized as follows. The second section describes integer-N frequency synthesizer PLL. The third section deals with loop filter design. Loop filter is most critical part for integration. In the fourth section is considered circuit implementation of PLL building blocks. Finally in the sections five conclusion is given.

2. PLL-BASED FREQUENCY SYNTHESIZER

Figure 1 depicts a PLL-based integer-N frequency synthesizer [1]. It consists of a phase-frequency detector (PFD), a charge-pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider (DIV). The output frequency is a multiple of the reference frequency if the loop is in the lock state:

$$f_{\text{out}} = N * f_{\text{ref}} \tag{1}$$

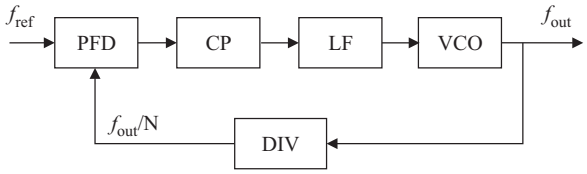

Fig.1. *Integer-N PLL-FS*

Frequency resolution is determined by referent frequency f_{ref}.

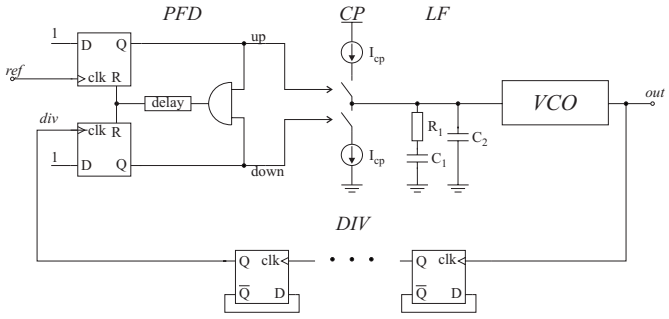

Fig.2. *Implementation of PLL-FS*

Fig. 2 presents a PLL-FS with some implementation details. The phase-frequency detector detects the phase and frequency difference between the reference and the feedback signal. The charge pump transfers the phase difference into current. A passive second order loop filter is used. C_1 and R_1 are used to generate zero for stability. C_2 is used to smooth the VCO control voltage ripples and to generate second pole. If N is a power of two, a simple divider consisting of T flip-flops can be used.

Fig. 3 gives the linear phase (noise) model of PLL-FS. The PFD and charge pump are combined in one block. Phase noise generated by each building block is referred to its output.

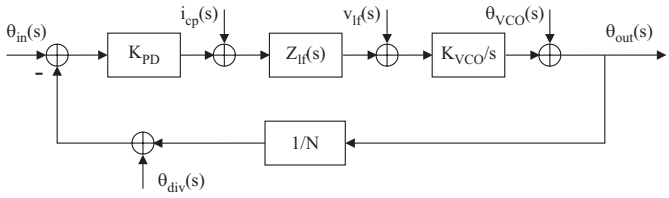

Fig.3. *PLL-FS linear model*

Notations are:

$\theta_{\text{in}}(s)$: input phase noise.

$i_{\text{cp}}(s)$: current noise associated with PFD and CP.

$v_{\text{lf}}(s)$: loop filter voltage noise

$\theta_{\text{VCO}}(s)$: VCO output phase noise

$\theta_{\text{out}}(s)$: PLL output phase noise

$\theta_{\text{div}}(s)$: divider phase noise

$K_{\text{PD}}(s)$: PFD and CP gain, equal to $I_{\text{cp}}/2\pi$ [A/rad]

$Z_{\text{lf}}(s)$: loop filter transimpedance

$K_{\text{VCO}}(s)$: VCO conversion gain [rad/s/V]

N: frequency division ratio

I_{cp}: charge pump current

Open loop phase transfer function is:

$$H_{\text{ol}}(s) = \frac{K_{\text{VCO}} I_{\text{cp}}}{2\pi s N} Z_{\text{lf}}(s) \tag{2}$$

Due to the inherent pole at origin provided by VCO, the PLL is always one order higher than the loop filter.

3. LOOP FILTER DESIGN

As mentioned in section 2 loop filter is used to smooth the VCO control voltage. To ensure stability of the loop and to remove spurs from reference bandwidth of the closed loop filter is constrained to $f_{\text{ref}}/10$ [2].

Transimpedance of a second order filter can be expressed as:

$$Z_{lf}(s)=\left(\frac{b}{b+1}\right)\frac{\tau s+1}{sC_1\left(\frac{\tau s}{b+1}+1\right)} \tag{3}$$

where $\tau = R_1C_1$ and $b = C_1/C_2$. The open loop transfer function of the third-order PLL is:

$$H_{ol}(s)=\frac{K_{VCO}I_{cp}}{2\pi}\left(\frac{b}{b+1}\right)\frac{\tau s+1}{s^2C_1\left(\frac{\tau s}{b+1}+1\right)} \tag{4}$$

The phase margin of the loop is

$$PM = \tan^{-1}(\tau\omega_c)-\tan^{-1}\left(\frac{\tau\omega_c}{b+1}\right) \tag{5}$$

where ω_c is the PLL open loop crossover frequency (unity gain frequency). Open loop crossover frequency and bandwidth of the PLL close loop transfer function have almost same values and crossover frequency is used as bandwidth of the PLL closed loop. Finding the extremum of PM with respect to ω_c gives [3]:

$$\omega_c = \sqrt{b+1}/\tau \tag{6}$$

and the maximum phase margin is

$$PM_{max} = \tan^{-1}\left(\sqrt{b+1}\right)-\tan^{-1}\left(\frac{\sqrt{b+1}}{b+1}\right). \tag{7}$$

The maximum phase margin is exclusively determined by the capacitor ratio *b*.

Matlab [4] is used to plot equatations (5) and (6) Results are shown in Fig. 4. Solid line represent constant phase margin while dashed line represent maximum of phase margin in respect to $\tau\omega_c$. It should be noted that the actual benefit of positioning loop filter at the phase margin extreme is minimized sensitivity of PM to variations of design parameters. Variation of $\tau\omega_c$ and *b* don't have significant influence on phase margin as can be observed from Fig 4. Capacitor ratio can be controlled accurately while absolute values for capacitance and resistance have variation is typically 10%-20%, while variation of K_{VCO} can be more then a factor of 2.

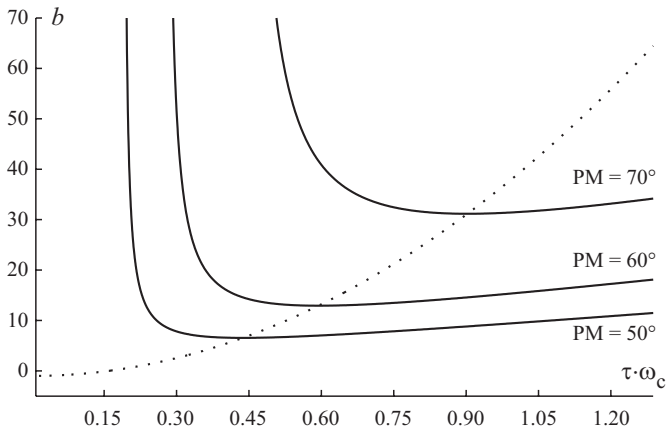

Fig.4. Implementation of PLL-FS

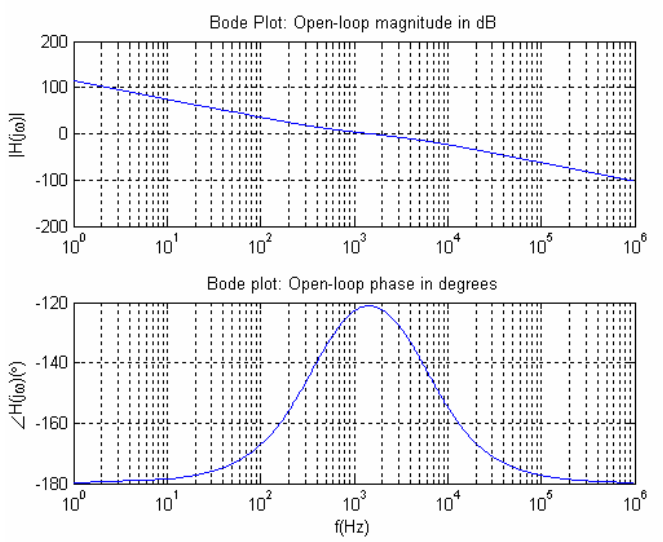

Fig. 5 PLL *Open-loop gain and phase*

Therefore, we have to keep enough phase margin to accommodate variations of design parameters. Matlab is used to solve needed equations and calculate loop filter values.

For given f_c of 1500 Hz, phase margin of 60°, K_{VCO} of 12.4 MHz/V, charge pump current of 15 µA an division ratio of 128 calculated and rounded to the closest standard values for R_1, C_1, C_2 are 6.8 kΩ, 56nF and 4.7nF respectively. Obtained values are too big for integration and must be placed off chip.

PLL open-loop gain and phase are shown in Fig. 5, while in Fig. 6 are depicted closed loop transfer functions. To ensure that variation of f_c do not decrease phase margin significantly in Fig. 7 is plotted phase margin variation due to variation of the f_c. Phase noise simulation is done with SpecreRF [5] simulator. Instead to simulate phase noise for whole PLL each block is simulated and Matlab is used to combine phase noise contribution from each block to obtain phase noise for whole PLL. This is done to reduce time for phase noise analysis [6]. Result is shown in Fig. 8. VCO phase noise is dominant as can be seen from Fig. 8.

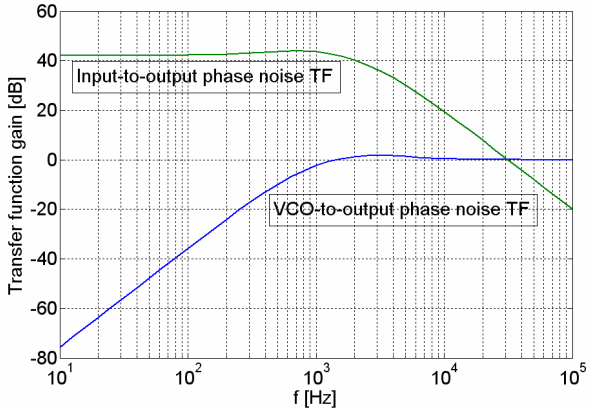

Fig. 6 *PLL closed-loop phase transfer function*

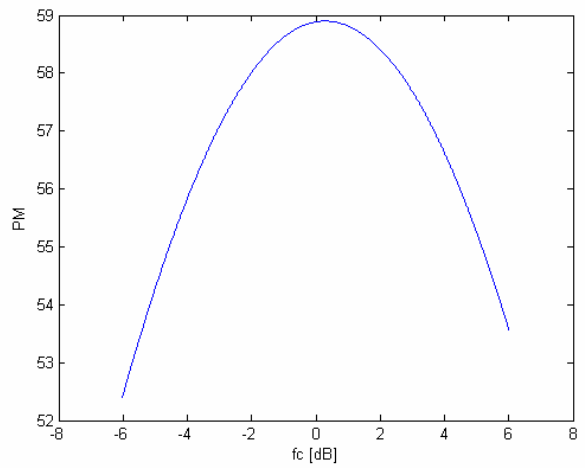

Fig 7 *Phase margin variation with respect to* f_c

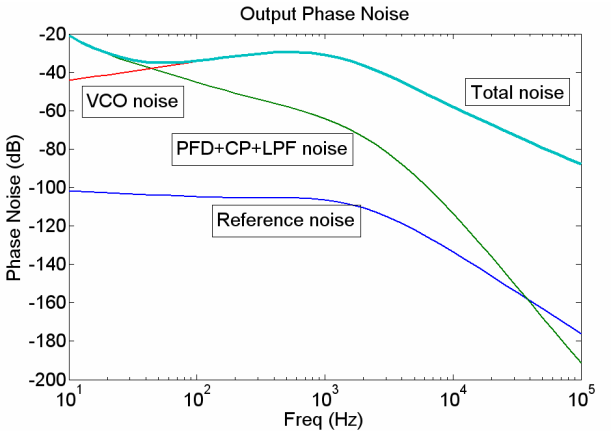

Fig. 8 *Phase noise*

To integrate loop filter on chip values for C_1, C_2 must be smaller. For a given bandwidth ω_c and loop zero ω_z products $I_{cp}C_1$ and R_1C_1 are fixed. To reduce the size of C_1 we need to increase R_1 and hence to decrease I_{cp}. However, phase noise introduced by both I_{cp} and R_1 increase in doing so. For PLL parameters f_c of 2000 Hz, phase margin of 50°, K_{VCO} of 4 MHz/V, charge pump current of 1 μA and division ratio of 128 using Matlab we obtain values for R_1, C_1, C_2. The new values for C_1 and C_2 are too big to be placed on chip so it must be modified Modifying values of C_1 and C_2 phase margin maximum is not achieved for f_c and phase margin is more sensitive to f_c variation as can be seen from Fig. 9. The modified values are 400 kΩ, 400pF and 10pF respectively. C_1 value is still large for integration and capacitance multiplier circuit [7] is used (Fig. 10) to obtain desired capacitance with multiplication factor of 20 (N=19). Higher multiplication ratios can be achieved at the cost of increased power dissipation (current is N times larger). Closed-loop transfer function is shown in Fig. 11.

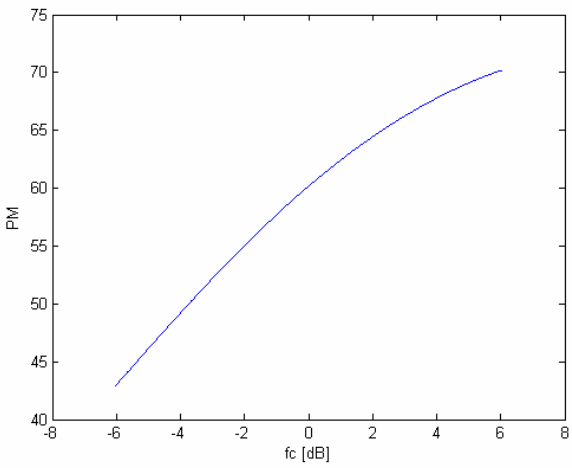

Fig. 9 *Phase margin variation with respect to* f_c

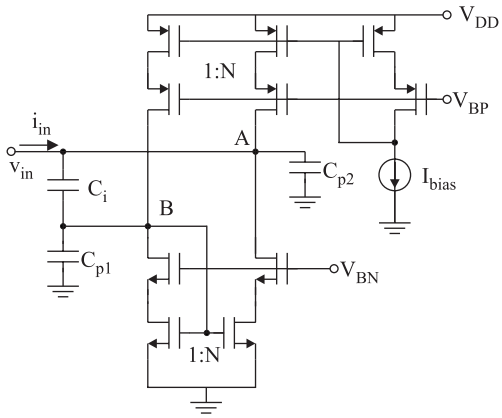

Fig. 10. *Capacitance multiplier*

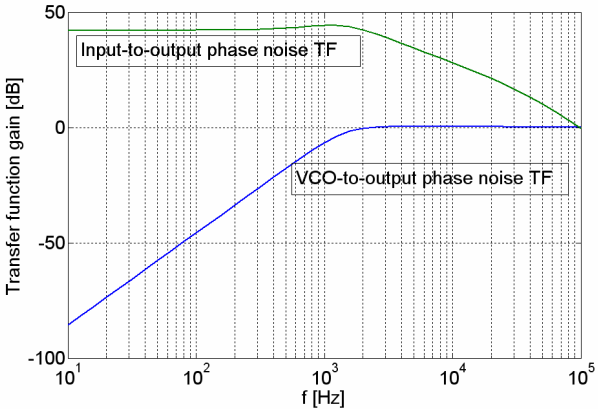

Fig. 11 *PLL closed-loop phase transfer function*

4. CIRCUIT IMPLEMENTATION

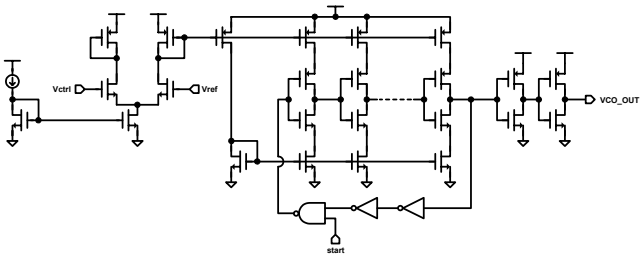

Fig. 12 *Current starved ring oscillator*

Phase detector is implemented as dead-zone free PFD [8] as shown Fig. 2. VCO is current starved ring oscillator as shown in Fig. 12. From transistor level simulation VCO transfer characteristic is derived (Fig. 13). We need to convert control voltage into current. This can be done with differential par as shown to the left in Fig. 12 or if we need wide range of control voltage circuit shown in Fig. 14 can be used. Capacitor is added for stability.

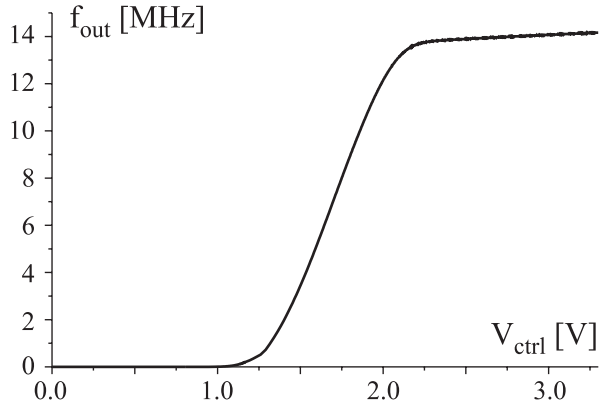

Fig. 13 *VCO transfer characteristic*

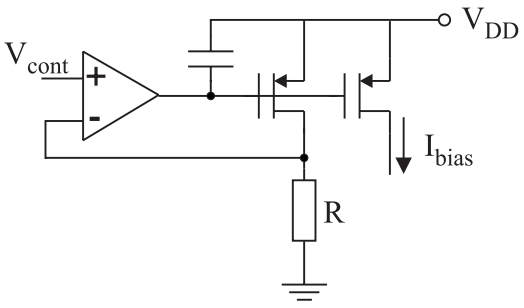

Fig. 14 Voltage to current convertor

5. CONCLUSION

In this paper we represent design considerations for 4.19 MHz PLL from 32 kHz reference in standard CMOS technology. Due to low bandwidth of PLL loop required values for loop filter are too big for integrated on chip. An attempt to integrate loop filter is made using capacitance multiplier to obtain bigger capacitance values. Penalty for integrating loop filter is area overhead and increased noise.

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Abstract – U ovom radu je dat postupak projektovanja 4.19 MHz PLL-a sa referentnom frekvencijom od 32 KHz u standardnoj CMOS tehnologiji sa niskofrekventnim filtrom implementiranim van čipa. Takođe, razmatrana je i integracija niskopropusnog filtra na čipu i predloženo je jedno rešenje.

PROJEKTOVANJE SINTETIZATORA FREKVENCIJE U CMOS TEHNOLOGIJI

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